CLAIMS

What is claimed is:

1. A computerized method for generating test instruction sequences, the method comprising:

identifying a plurality of operation codes, the plurality of operation codes included in an instruction set supported by a processor;

identifying a plurality of registers, the plurality of registers associated with the processor;

generating a plurality of test instructions, the test instructions generated by combining fragments associated with the plurality of operation codes and registers; and

generating a plurality of check instructions, the check instructions configured to determine if the test instructions are run correctly.

2. The computerized method of claim 1, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a programmable chip.

3. The computerized method of claim 1, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a central processing unit.

4. The computerized method of claim 1, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a digital signal processor.

5. The computerized method of claim 1, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, and operands.

6. The computerized method of claim 1, wherein the plurality of test instructions and check instructions are used to test an assembler.

7. The computerized method of claim 2, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, operands, and expected operation codes.

8. The computerized method of claim 7, wherein the expected operation codes identify the operation the assembler should perform.

9. The computerized method of claim 1, further comprising identifying configuration information for limiting the set of generated test instructions.

10. The computerized method of claim 9, wherein configuration is provided by a user to narrow generated test instructions to particular operations or registers.

11. The computerized method of claim 1, wherein the plurality of test instructions and check instructions are generated by identifying associated bit fragments.

12. A system for generating test instruction sequences, the system comprising:

means for identifying a plurality of operation codes, the plurality of operation codes included in an instruction set supported by a processor;

means for identifying a plurality of registers, the plurality of registers associated with the processor;

means for generating a plurality of test instructions, the test instructions generated by combining fragments associated with the plurality of operation codes and registers; and

means for generating a plurality of check instructions, the check instructions configured to determine if the test instructions are run correctly.

13. The system of claim 12, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a programmable chip.

14. The system of claim 12, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a central processing unit.

15. The system of claim 12, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, and operands.

16. The system of claim 12, wherein the plurality of test instructions and check instructions are used to test an assembler.

17. The system of claim 13, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, operands, and expected operation codes.

18. The system of claim 17, wherein the expected operation codes identify the operation the assembler should perform.

19. The system of claim 12, further comprising identifying configuration information for limiting the set of generated test instructions.

20. The system of claim 19, wherein configuration is provided by a user to narrow generated test instructions to particular operations or registers.

21. The system of claim 12, wherein the plurality of test instructions and check instructions are generated by identifying associated bit fragments.

22. A computer readable medium comprising computer code for generating test instruction sequences, the computer readable medium comprising:

computer code for identifying a plurality of operation codes, the plurality of operation codes included in an instruction set supported by a processor;

computer code for identifying a plurality of registers, the plurality of registers associated with the processor;

computer code for generating a plurality of test instructions, the test instructions generated by combining fragments associated with the plurality of operation codes and registers; and

computer code for generating a plurality of check instructions, the check instructions configured to determine if the test instructions are run correctly.

23. The computer readable medium of claim 22, wherein the plurality of test instructions and check instructions are used to test a processor core associated with a programmable chip.

24. The computer readable medium of claim 22, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, and operands.

25. The computer readable medium of claim 22, wherein the plurality of test instructions and check instructions are used to test an assembler.

26. The computer readable medium of claim 23, wherein ones of the plurality of test instructions and check instructions generated to test the assembler include operation codes, operands, and expected operation codes.

27. The computer readable medium of claim 26, wherein the expected operation codes identify the operation the assembler should perform.

28. The computer readable medium of claim 22, further comprising identifying configuration information for limiting the set of generated test instructions.

29. The computer readable medium of claim 28, wherein configuration is provided by a user to narrow generated test instructions to particular operations or registers.

30. The computer readable medium of claim 22, wherein the plurality of test instructions and check instructions are generated by identifying associated bit fragments.